## REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

The specification, including the abstract, has been editorially revised to place the application in better form for issue.

Claims 1-4 and 20 have been amended. Claims 16-19 have been cancelled without prejudice or disclaimer, and Claims 22-46 stand withdrawn from consideration. New Claim 47 has been added and is readable on the elected species. Accordingly, Claims 1-15, 20-21, and 47 are subject to further examination.

The Office Action rejected Claims 1-21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,227,339 to Kishii in view of JP 2000-150640 to Hidemitsu.

Without acceding to the rejection, each of independent Claims 1-3 has been amended more particularly to set forth certain distinctive features of Applicants' invention. At least as presently amended, Claims 1-3 distinguish patentably from the collective teachings of Kishii and Hidemitsu.

The claimed invention relates to an improved method of semiconductor device manufacture which can reduce the deleterious effects of substrate charge-up which occurs as a

result of plasma treatment. See the introductory portion of Applicants' specification at pages 1-5. In accordance with Applicants' invention, the manufacturing method of a semiconductor device comprises a step of forming a first insulating film on a first main surface of a substrate, and a step of forming a second insulating film on the substrate. The second insulating film may be formed on a second main surface of the substrate (Claim 1), a bevel portion of the substrate (Claim 2), or both a second main surface and a bevel portion of the substrate (Claim 3). The method additionally comprises a step of polishing a surface of the first insulating film through a CMP method to remove particles disposed on the first insulating film after the step of forming the second insulating film. Note, for example, the discussion in the first full paragraph on page 24 of the specification. A wiring layer is thereafter formed over the first main surface of the substrate through a plasma treatment.

The collective teachings of Kishii and Hidemitsu neither disclose nor suggest Applicants' claimed invention as described above.

Kishii discloses a method by which one of the wafers in a substrate having an SOI structure composed of two semiconductor substrates bonded through an insulating layer

can be formed to a uniform thickness of a few micrometers or less. Specifically, and with reference to Figs. 10A-E of Kishii, an oxide film 22 is formed on the surface of at least one of the two wafers 20-21. Then, the silicon wafers 20 and 21 are overlapped so that the polished surfaces thereof confront or are in contact with each other and are subjected to a heat treatment. To increase a bonding force, a method of imposing a pulse voltage between the silicon wafer 20, 21 prior to the heat treatment is known. Therefore, the silicon wafer 20 is strongly bonded to the silicon wafer 21 through the oxidized film 22.

However, Kishii fails to teach or suggest the combined insulating film forming steps and CMP polishing step as outlined above. Furthermore, Kishii fails to teach or suggest the forming of a wiring layer over the first main surface through plasma treatment after the polishing step as claimed.

Hidemitsu fails to overcome the deficiencies as noted above in relation to Kishii. Hidemitsu discloses the ability to prevent degradation of device characteristics and current leakage due to metal contaminants such as copper or a copper compound, from adhering to the reverse side of a semiconductor substrate. In particular, a copper base metal film is formed on the major surface of the semiconductor

substrate after forming a barrier film on the reverse side of the semiconductor substrate. However, Hidemitsu fails to teach at least the step of polishing the surface of the first insulating film through a CMP method to remove particles disposed thereon after the step of forming of the second insulating film as claimed. Nor does Hidemitsu suggest the necessity of such step.

As the collective teachings of Kishii and Hidemitsu thus fail to suggest Applicants' invention as claimed, it is respectfully urged that the outstanding rejection under § 103(a) be withdrawn and that this application be passed to issue.

An early Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this

paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

_____ November 19, 2003
Mitchell W. Shapiro Date